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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,901	10/29/2003	Cesar H. Proano	005513.P015	9235
7590 Daniel E. Ovanezian BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP Seventh Floor 12400 Wilshire Boulevard Los Angeles, CA 90025-1026	03/02/2007		EXAMINER RAHMJOO, MANUCHER	
			ART UNIT 2624	PAPER NUMBER

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/697,901	PROANO ET AL.
	Examiner	Art Unit
	Mike Rahmjoo	2624

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 12/29/03.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-27 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-27 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____

5) Notice of Informal Patent Application

6) Other: _____

DETAILED ACTION

Claim Objections

Claim 3 is objected to because of the following informalities:

Claim 3 has incorrect dependency. To expedite current prosecution examiner will assume said dependency to be of claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 13 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As per claim 13 applicant claims "the second signal generator is configured to drive a first charge through the side opposite that of the plurality of electrodes into the plurality of storage capacitors, and wherein the first signal generator is coupled to the conductive structure to drive a second charge through the insulator". As per applicant's paragraph [0033] of specification, applicant teaches "a second pulse 495 may be applied directly to the storage capacitors (e.g., capacitors 140, 142, and 144) of

scanner 100 such that the sensing circuits 180 (e.g., capacitors 140, 142 and 144) store charge driven through finger 110 and also a constant charge due to pulse 495". Examiner fails to see any teachings of a second signal generator as being claimed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1- 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Bir et al (US Patent 6108438), hereinafter, Bird.

As per claim 1 Bird teaches an insulator having a bottom surface corresponding to for example fig. 3 block 15;

a pixel array coupled to the insulator corresponding to for example fig. 3 block 33. At the time the invention was made, it would have been obvious to incorporate pixel array coupled to the bottom surface of the insulator because applicant does not disclose said feature as providing an advantage, is used for a particular purpose or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected applicant's invention to perform with pixel array coupled to surfaces other than the bottom surface of the insulator;

a conductive structure adjacent to the pixel array corresponding to for example fig. 1 block 18 and 20;

and a first signal generator coupled to the conductive structure corresponding to for example column 6 line 47.

As per claim 2 Bird teaches the pixel array comprises amorphous silicon (a-Si) transistors corresponding to for example column 5 line 35.

As per claim 3 Bird teaches the a-Si pixel array is the basis for a thin film transistor ("TFT") flat panel detector corresponding to for example column 10 line 10.

As per claim 4 Bird teaches the conductive structure is configured to reside underneath a contacting portion of a hand corresponding to for example fig. 3 and column 9 lines 53- 55 wherein strips of conductive material may be provided directly on the upper surface of the insulating layer 25

As per claim 5 Bird teaches the first signal generator is configured to drive a charge through the insulator corresponding to for example column 6 lines 50- 57 wherein various potential and driving schemes are used.

As per claim 6 Bird teaches the first signal generator generates a pulse corresponding to for example column 6 lines 47 wherein a pulse is generated.

As per claim 7 Bird teaches the pulse has a negative potential corresponding to for example column 9 line 29 through the application of negative voltage pulse.

As per claim 8 Bird teaches the first signal generator generates a signal that changes its voltage amplitude corresponding to for example column 9 line 33 wherein the voltage is returned to zero from a negative value.

As per claim 9 Bird teaches a plurality of electrodes coupled to the insulator corresponding to for example fig. 3 blocks 33;

and a plurality of storage capacitors, each of the plurality of storage capacitors coupled to a corresponding one of the plurality of electrodes corresponding to for example fig. 3 blocks 35; and a second signal generator coupled to the plurality of storage capacitors on a side opposite that of the plurality of electrodes corresponding to for example fig. 2- 7 and column 6 line 46 wherein each amplifier is connected to a pulse generation circuit within the sense circuit and column 10 lines 30 35 wherein the array is driven by plurality of pulse signals.

As per claim 10 Bird teaches the second signal generator is configured to drive a charge directly into the plurality of storage capacitors through the side opposite that of the plurality of electrodes corresponding to for example column 10 lines 30- 35 wherein the array is driven by plurality of pulse signals including a first positive pulse and a negative pulse signal.

As per claim 11 Bird teaches the second signal generator generates a pulse corresponding to for example column 10 lines 30- 35 wherein plurality of pulse signals including a first positive pulse and a negative pulse signal exist.

As per claim 12 Bird teaches the pulse has a negative potential corresponding to for example column 10 line 33.

As per claim 13 Bird teaches the second signal generator is configured to drive a first charge through the side opposite that of the plurality of electrodes into the plurality of storage capacitors, and wherein the first signal generator is coupled to the

conductive structure to drive a second charge through the insulator corresponding to for example column 9 lines 45- 50 wherein the voltage pulses applied to the column conductors 20 could be provided by a separate circuit connected to the column conductors, for example at their ends remote from the column amplifiers 40, rather than via the amplifiers and also column 10 lines 10- 35 for the positive and negative selection pulses as corresponding to the first and second generation pulses.

As per claim 14 Bird teaches the conductive structure surrounds the pixel array corresponding to for example fig. 1 blocks 18 and 20.

As per claim 15 Bird teaches fingerprint recognition system comprising the apparatus according to claim 1 corresponding to for example the title and device of fig. 1.

As per claim 16 and in light of the rejections made above Bird teaches a plurality of storage capacitors, each of the plurality of storage capacitors coupled to a corresponding one of the plurality of electrodes corresponding to for example fig. 3 and 5 and cap. 35 and 51;

driving a first charge through the finger into at least one of the plurality of storage capacitors corresponding to for example fig. 3 and 7 and column 10 lines 10- 35 for any of the positive and negative pulse signals as corresponding to first charge.

As per claim 17 Bird teaches the first charge is driven through the finger using a first pulse corresponding to for example column 6 lines 5-35 wherein the diodes are used to charge and discharge the capacitance formed between the finger portion and the sense electrode.

As per claim 18 Bird teaches the first pulse has a negative voltage corresponding to for example column 10 lines 10- 35 for the positive and negative selection pulses as corresponding to the first and second generation pulses.

As per claim 19 Bird teaches the first charge is driven into a first contact of the storage capacitor coupled to a corresponding electrode corresponding to for example fig. 3 capacitors 35 and the corresponding electrodes.

As per claim 20 Bird teaches driving a second charge into a second contact of the storage capacitor corresponding to for example fig. 3, 5 and 7 and column 10 lines 10- 35 for the positive and negative selection pulses as corresponding to the first and second generation pulses.

As per claim 21 Bird teaches the second charge is driven directly into the storage capacitor using a pulse corresponding to for example columns 7 and 10 lines 10- 35 for the positive and negative selection pulses as corresponding to the first and second generation pulses.

As per claim 22 Bird teaches the pulse has a negative voltage corresponding to for example column 10 lines 10- 35 for the negative selection pulses as corresponding to the first or second generation pulses.

As per claim 23 Bird teaches driving a second charge into a second contact of the storage capacitor, wherein the second charge is driven directly into the storage capacitor using a second pulse corresponding to for example column 10 lines 10- 35 for the positive and negative selection pulses as corresponding to the first and second generation pulses which is made through capacitors 35.

As per claim 24 Bird teaches the first pulse has a positive voltage column 10 lines 10- 35 for the positive selection pulses as corresponding to the first or second generation pulses.

As per claim 25 Bird teaches the first pulse has a voltage difference in the approximate range of 0.5V to 1V corresponding to for example column 8 lines 5- 67 through column 9 lines 1- 37 wherein the charge or voltage difference is about 1 volt (or higher) which is in accordance with applicant's disclosure in [0034].

Claims 26- 27 are substantially similar to claims 1- 24 and are rejected using the same rational.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PAP 2002/ 0156593

US Patent 5325442

Inquiry

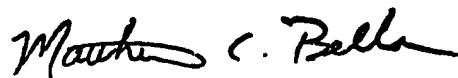
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Rahmjoo whose telephone number is 571-272-7789. The examiner can normally be reached on 8 AM- 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Bella can be reached on 571-272-7778. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mike Rahmjoo

February 26, 2007



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